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Silexica unveils SLX for FPGA Design Space Exploration to Optimize Hardware / Software Partitioning at Xilinx Developers Forum

- **Industry-first solution to analyze C/C++ code for RISC / FPGA design space exploration to optimize the hardware / software partitioning.**
- **Fully integrated with Xilinx SDSoC Development Environment and Vivado Design Suite for streamlined synthesis of SLX optimized code.**

SAN JOSE, California, Oct. 2, 2018 (Xilinx Developer Forum)– Silexica, (silexica.com) the makers of SLX programming tools for heterogeneous multicore devices, demonstrates the latest release of SLX for Xilinx Zynq-based devices with Arm processors. While analyzing C/C++ code for FPGA offload acceleration opportunities, the SLX FPGA flow identifies application hot spots that offer the greatest potential for increased system performance.

The SLX FPGA flow is complete with checks for C/C++ code synthesizability and estimates for the performance increases that are achievable by offloading software functions to the FPGA. Developers benefit from a single flow that can be used to optimize C/C++ for both the Arm Cortex-A processors and the FPGA fabric. The SLX FPGA flow delivers the industry's first complete C/C++ optimization solution that provides the user with deep insights into their application in order to guide the FPGA design space exploration to converge on optimized hardware / software.

This version of SLX was designed to support software professionals with a need to increase system performance by utilizing the FPGA for embedded computing tasks. Historically, identifying and optimizing C/C++ code for FPGA offloading has been difficult due to the lack

of a tool designed for analysis and optimization for both the RISC cores and FPGA fabric. SLX for FPGAs provides software developers a streamlined approach to optimize software for heterogeneous multicore systems. A live SLX version at the Silexica Booth showcases the workflow from C/C++ code analysis, and optimization, to FPGA code synthesis for the software identified by SLX as ideal for FPGA execution using the integrated SLX and Xilinx SDSoC flow.

"The convergence of multiple systems into a single device based on the Xilinx Zynq SoC introduces the daunting challenge of optimizing software from sources including commercial, 3rd party, community, and the semiconductor," said Maximillian Odendahl, CEO at Silexica. "This requires a new generation of tooling that can provide the deep insights into the software behavior that is required for system optimization and acceleration engine offloading which is exactly what SLX was designed for."

Silexica will be at three Xilinx Developer Forums in the Silicon Valley (US), Beijing (CN) and Frankfurt (DE). Silexica will be on stand 13 at the event in the Silicon Valley. Please contact us to arrange a meeting.

More information about XDF is available at: https://www.xilinx.com/products/design-tools/developer-forum/silicon-valley.html. For additional updates from XDF, follow Xilinx on Twitter at @XilinxInc or via the hashtag #XDF2018.

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About Silexica

Silexica provides software development solutions that enable technology companies to take intelligent products such as autonomous cars from concept to deployment. The SLX programming tools help developers implement software to run efficiently on embedded supercomputers by offering deep understanding of how software behaves on the system.

Silexica was founded in 2014 and has raised $28 million in funding. With headquarters in Germany and offices in the US and Japan, Silexica has partnered with global customers across many rapidly transforming industries including automotive, wireless and aerospace. For further information please visit: www.silexica.com