XDF XILINX DEVELOPER FORUM

AGENDA

October 1st | DAY 1

8:00 AM

Registration Open

9:00 AM - 5:30 PM

Developer Labs, Tutorials, and Tools Walkthroughs

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Xilinx Security Design Workshop

> Page 10

5:30 PM

Reception

October 2nd | DAY 2

7:00 AM

Registration Open

9:00 AM - 10:30 AM

Keynote: Victor Peng, President & CEO - Xilinx

10:45 AM - 11:45 AM

General Sessions

12:00 PM - 5:45 PM

Breakout Sesssions

Hardware Design

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Embedded System Software

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Edge Software Development

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Cloud Software Development

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Data Scientist / Frameworks

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Xilinx Security Design Workshop

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Exhibit Hall & Developer Hangouts

5:30 PM

Reception

*Updated 9/24 (Subject to change)

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Developer Labs and Sessions | **DAY 1**

9:00 AM - 5:30 PM

- **Session:** Xilinx Tools Overview
  Speaker: Ramine Roane
  VP Solutions Marketing
  Time: 9:15 AM - 10:00 AM

- **Session:** Meet The Experts: Vivado, IPI, HLS
  Speaker: Premduth Vidyanandan
  Director of Product Marketing - Vivado Tool Solutions
  Time: 10:15 AM - 1:15 PM

- **Lab:** Amazon EC2 F1 Instances Developer Lab
  Speaker: Thomas Bollaert
  Senior Technical Director - Software Applications
  Time: 10:15 AM - 12:45 PM
  Session Details

- **Lab:** Machine Learning for Embedded Lab
  Speaker: Andy Luo
  Sr. Product Marketing Manager - Machine Learning
  Time: (Session 1) 10:15 AM - 11:45 AM (Session 2) 2:00 PM - 3:30 PM
  Session Details

- **Lab:** Model-Based Design with Xilinx Model Composer and Simulink (Hands-on Labs)
  Speaker: Uttara Kumar
  Product Marketing Manager - System Generator & Model Composer
  Time: 10:15 AM - 1:15 PM
  Session Details

- **Lab:** Introduction to Ultra96 and Xilinx Embedded Software
  Speaker: Tom Curran
  Avnet
  Time: 10:15 AM - 11:45 AM
  Session Details

- **Lab:** Building Vision System Using ML + CV + Sensors with SDSoC
  Speaker: Rob Armstrong
  Sr. Product Marketing Manager - Xilinx
  Time: (Session 1) 11:45 AM - 1:15 PM
  (Session 2) 3:30 PM - 5:00 PM
  Session Details

- **Lab:** Introduction to Software Acceleration with SDSoC
  Speaker: Dan Rozwood
  Sr. Technical Marketing Engineer, EM - Avnet
  Time: 11:45 AM - 1:15 PM
  Session Details

- **Session:** Conversation with Xilinx Research Labs
  Speaker: Ivo Bolsens
  CTO and Sr. Vice President
  Time: 12:00 PM - 2:00 PM
  Session Details

- **Session:** Accelerate FPGA Development, Test and Application Deployment Natively on AWS EC2 F1
  Speaker: Kris King
  Design Verification Manager - Silicon Optimization – AWS
  Time: 1:30 PM - 2:15 PM
  Session Details

- **Lab:** Open CV Acceleration
  Speaker: Yashu Gosain
  Sr. Manager SoC Technical Marketing - MPSoC Multimedia
  Time: 2:00 PM - 3:30 PM
  Session Details

- **Session:** Accelerating Hadoop Map-Reduce on F1 and Achieving 10X Speed-up!
  Speaker: Abhishek Ranjan and Mohit Kumar
  Co-Founders - BigZetta Systems
  Time: 2:15 PM - 2:45 PM
  Session Details

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Developer Labs and Sessions | **DAY 1**

9:00 AM - 5:30 PM

- **Session:** Addressing the Ease-of-Deployment and Monetization Challenges for Cloud and on-premise: How to Further Accelerate the Adoption of FPGAs in Data Centers
  Speaker: Stephane Monboisset
  VP Marketing & Partnerships - Accelize
  Time: 2:45 PM - 3:15 PM
  Session Details

- **Session:** AI Developer Lab with Xilinx ML Suite for DC / Cloud
  Speaker: Kamran Khan
  Product Marketing Manager - Libraries and Software Acceleration
  Time: 3:30 PM - 5:30 PM
  Session Details

- **Session:** Python on Zynq UltraScale+ Showcasing OpenCV Libraries
  Speaker: Forrest Pickett
  Sr. SoC Solutions Line Manager
  Time: 3:30 PM - 5:00 PM
  Session Details

- **Session:** FPGA Accelerated Genomics Analysis
  Speaker: Rami Mehio
  Senior Director of Engineering - Illumina
  Time: 4:15 PM - 4:45 PM
  Session Details

- **Session:** Accelerate Real-Time High Definition Video Processing Designs with Digilent Zybo Z7, a Zynq-7000 AP SoC Platform and Xilinx Vivado HLS
  Speaker: Thomas Kappenman
  Application Engineer - Digilent
  Time: 2:00 PM - 5:30 PM
  Lab Requirements: Windows 7 at minimum, Vivado Design Suite HLx Edition 2018.1, HLS 2018.1 and SDK 2018.1 Installed

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Hardware Design | **DAY 2**

This track is intended for hardware designers and system architects who want to learn best practices in using Vivado (timing, synthesis, partial reconfiguration), HLS/IPI, Model Composer and other tools. It will consist of sessions conducted by Xilinx technologists, guest speakers, and conclude with an expert panel discussion and Q&A. This popular track is suited for hardware designers using FPGAs for a wide variety of traditional FPGA applications.

12:00 PM - 5:45 PM

- **Session:** IPI Methodology
  Speaker: Daniel Michek
  Product Marketing Manager - HLx Design Tools
  Time: 12:00 PM - 12:45 PM

- **Guest Session:** FPGA Design with the Cloud From Simple Compliation to Timing Optimization
  Speaker: Kirvy Teo
  Co-Founder - Plunify
  Time: 12:15 PM - 12:45 PM
  > Session Details

- **Session:** HLS Tips and Tricks
  Speaker: Frederic Rivoallon
  Product Manager - SDAccel and Vivado HLS
  Time: 12:45 PM - 1:30 PM
  > Session Details

- **Session:** RTL Synthesis Methodology
  Speaker: Balachander Krishnamurthy
  Sr. Product Marketing Manager
  Time: (Session 1) 1:00 PM - 1:45 PM
  (Session 2) 2:45 PM - 3:30 PM
  > Session Details

- **Session:** Revision Control Methodology
  Speaker: Brian Lay
  Product Marketing Manager - Vivado
  Time: 1:45 PM - 2:30 PM
  > Session Details

- **Session:** Timing Closure Tips and Tricks
  Speaker: Ron Plyer
  Product Marketing Manager - Physical Implementation Tools
  Time: 45 Minutes | (Session 1) 2:00 PM - 2:45 PM
  (Session 2) 3:45 PM - 4:30 PM
  > Session Details

- **Session:** Partial Reconfiguration: Methodologies for Creating Reconfigurable Applications
  Speaker: David Dye
  Sr. Product Marketing Engineer
  Time: 3:00 PM - 3:45 PM
  > Session Details

- **Guest Session:** Visual System Integrator (VSI): An Environment for Rapid Development & Integration of Heterogenous Systems
  Speaker: Sandeep Dutta
  CEO - SystemView Inc.
  Time: 4:00 PM - 4:45 PM
  > Session Details

- **Expert Panel:** Hardware Design and Vivado
  Host: Premduth Vidyanandan
  Director of Product Marketing - Vivado Tool Solutions
  Time: 4:45 PM - 5:30 PM

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Embedded System Software | **DAY 2**

This track is intended for developers of software for embedded systems who want to hear about best practices for heterogeneous runtime design. Technical content in this track will cover open source OS and hypervisor considerations as well as multimedia and platform management. Discussions in this track will focus on ARM-based Xilinx SoC and RFSoC platforms.

12:00 PM - 5:45 PM

- **Session:** Embedded Software Strategy & Development, an Introduction
  Speaker: Tony McDowell
  Sr. Product Marketing Engineer 2 - SoC Runtime Software
  Time: 1:00 PM - 1:45 PM
  Session Details

- **Session:** Heterogenous Realtime Software Architecture
  Speaker: Stefano Stabellini
  System Software Architect
  Time: 2:00 PM - 2:45 PM
  Session Details

- **Session:** SoC Platform Management
  Speaker: Jerry Wong
  SoC Technical Marketing - MPSoC Power
  Time: 3:00 PM - 3:45 PM
  Session Details

- **Session:** From DC to Daylight, Xilinx RF Solutions for Wired, Wireless and High Frequency Applications
  Speaker: Glenn Steiner
  Sr. Manager - SoC Technical Marketing, MPSoC Power, Functional Safety & Applications

  Speaker: David Brubaker
  Sr. Product Line Manager
  Time: 3:45 PM - 5:15 PM
  Session Details

- **Session:** Multimedia SoC System Solutions
  Speaker: Yashu Gosain
  Sr. Manager SoC Technical Marketing - MPSoC Multimedia
  Time: 4:00 PM - 4:45 PM
  Session Details

- **Session:** Bringing the Benefits of Cortex-M Processors to FPGA
  Speaker: Michele Riga
  Product Manager, Embedded and Automotive - Arm

  Speaker: Simon George
  System Software and SoC Solution Marketing - Xilinx
  Time: 5:00 PM - 5:45 PM
  Session Details

- **Guest Session:** System Design from Antenna to Digital with Zynq UltraScale+ RFSoC
  Speaker: Luc Langlois
  Director, Engineering & Technology / Digital Signal Processing - Avnet
  Time: 5:15 PM - 5:45 PM
  Session Details

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Edge Software Development | **DAY 2**

This track is intended for software application developers and system architects who are designing accelerated systems on the edge – in automotive, smart city, machine vision and more. Emphasis will be on intelligent vision applications, leveraging accelerated computer vision and/or machine learning inference. SDSoC tools and CV libraries will be discussed in addition to machine learning stack and tools (pruning, compression, quantization) from DeePhi. Target platforms for this track will be focused on Xilinx Zynq SoC.

12:00 PM - 5:45 PM

- **Repeat Session:** Xilinx Machine Learning Strategies with DeePhi Acquistion
  Speaker: Nick Ni
  Director of Product Marketing - Xilinx

  Speaker: Yi Shan
  Sr. Director of Engineering - DeePhi
  Time: 12:00 PM - 1:00 PM
  > Session Details

- **Lab:** Design and Deploy Accelerators for Embedded Vision Systems using Model Composer and SDSoC
  Speaker: Uttara Kumar
  Product Marketing Manager - System Generator & Model Composer
  Time: 12:00 PM - 1:30 PM
  > Session Details

- **Session:** Accelerating ADAS Computer Vision Application Development at Ford using SDSoC
  Speaker: Vijay Nagasamy
  Research Scientist, Autonomous Vehicles - Ford Greenfield Labs
  Time: 1:00 PM - 1:30 PM
  > Session Details

- **Workshop:** Machine Learning for Embedded
  Speaker: Jingxiu Liu
  Director of Product Marketing - DeePhi
  Time: 1:45 PM - 3:15 PM
  > Session Details

- **Repeat Session:** Machine Learning for Embedded Deep Dive
  Speaker: Andy Luo
  Sr. Product Marketing Manager, Machine Learning - Xilinx

  Speaker: Jingxiu Liu
  Director of Product Marketing - DeePhi
  Time: 2:00 PM - 3:00 PM
  > Session Details

- **Repeat Session:** Using Machine Learning with SDSoC to Create Embedded Vision Systems
  Speaker: Rob Armstrong
  Sr. Product Marketing Manager
  Time: 3:15 PM - 4:15 PM
  > Session Details

- **Workshop:** Building Vision System using ML + CV + Sensors w/SDSoC
  Speaker: Rob Armstrong
  Sr. Product Marketing Manager
  Time: 3:30 PM - 5:00 PM
  > Session Details

- **Session:** Expert Panel for Edge Computing: ML, OpenCV, SDSoC, Sensor Fusion
  Speaker: Nick Ni
  Director of Product Marketing - Artificial Intelligence and Edge Computing
  Time: 4:30 PM - 5:00 PM
  > Session Details

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Cloud Software Development | **DAY 2**

This track is intended for application developers and system architects who are designing accelerated applications in the data center or cloud – for data analytics, financial, genomics, video streaming and more. Emphasis will be on development and deployment with SDAccel and compute acceleration libraries that form the software acceleration stack for high performance Xilinx Virtex FPGAs used in cloud and on-premise data centers. Cloud FPGA computing services like AWS F1 as well as data center hardware accelerator platforms will be covered.

12:00 PM - 5:45 PM

- **Session:** State of FPGA-based Acceleration
  Speaker: Vinay Singh
  Sr. Director Solutions and Platform Marketing - SW Development Environments, DC and Edge Solutions
  Time: 12:00 PM - 12:30 PM
  Session Details

- **Session:** Video Acceleration in the Cloud Using FPGAs
  Speaker: Sean Gardner
  Sr. Marketing Manager - Video Acceleration

  Speaker: Johan Janssen
  Chief Video Architect and Sr. Director of Video IP Solutions - Xilinx
  Time: 12:00 PM - 12:30 PM
  Session Details

- **Session:** Converged IO Acceleration Platform
  Speaker: Ravi Sunkavalli
  Vice President - IP Engineering
  Time: 12:00 PM - 12:30 PM
  Session Details

- **Session:** Empowering Software Developers - Scaling FPGA Application Development
  Speaker: Dan Gibbons
  Vice President - Interactive Design Tools
  Time: 12:30 PM - 1:15 PM
  Session Details

- **Session:** The Nuts & Bolts of Computational Storage Platform
  Speaker: Gopi Jandhyala
  Senior Director - IP Solutions
  Time: 12:30 PM - 1:00 PM
  Session Details

- **Session:** Developing Computational Storage Applications using SDAccel
  Speaker: Sumit Roy
  Sr. Engineering Director - Xilinx
  Time: 1:00 PM - 1:30 PM
  Session Details

- **Session:** Fundamentals of FPGA based Acceleration
  Speaker: Thomas Bollaert
  Sr. Technical Director - Software Applications
  Time: 2:00 PM - 2:45 PM
  Session Details

- **Session:** Using SD Accel for Host and Accelerator Code Optimizations
  Speaker: Peter Frey
  Xilinx
  Time: 3:30 PM - 5:00 PM
  Session Details

- **Session:** SDAccel - Ask the Experts Panelists and Wrap-up
  Speaker: Vinay Singh
  Sr. Director Solutions and Platform Marketing - SW Development Environments, DC and Edge Solutions
  Time: 5:00 PM - 5:30 PM

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Cloud Software Development | **DAY 2**

12:00 PM - 5:45 PM

- **Guest Session:** Best-in-Class Video Compression Developed with High Level Synthesis and SDAccel
  Speaker: Adam Malamy
  VP of Technology - NGCodec
  Time: 12:30 PM - 1:00 PM
  Session Details

- **Guest Session:** Building and Scaling FPGA Accelerated Applications for Cloud Computing
  Speaker: Steve Hebert
  CEO - Nimbix
  Time: 1:15 PM - 1:45 PM
  Session Details

- **Guest Session:** Building Next-Generation Accelerated Video and Machine Learning Software Solutions Running on the Xilinx Virtex UltraScale+
  Speaker: Marc Todd
  Founder & CEO - Skreens
  Time: 1:45 PM - 2:15 PM
  Session Details

- **Guest Session:** FPGAs - Moving Computation to the Data
  Speaker: John Davis
  Chief Product Officer - BigStream
  Time: 1:45 PM - 2:15 PM
  Session Details

- **Guest Session:** API for Real Time / Dynamic Image Processing
  Speaker: Harry Yu
  CEO - CTAccel
  Time: 2:15 PM - 2:45 PM
  Session Details

- **Guest Session:** Computational Storage - Acceleration Through Intelligence & Agility
  Speaker: Thad Omura
  EVP Marketing - Scaleflux
  Time: 2:15 PM - 2:45 PM
  Session Details

- **Guest Session:** SDAccel Development Environment: FPGA Acceleration Performance and Ease of Use Aren't Mutally Exclusive
  Speaker: Pat McGarry
  Vice President of Engineering - BlackLynx
  Time: 2:45 PM - 3:30 PM
  Session Details

- **Session:** Financial Analytics Acceleration
  Speaker: Oskar Mencer
  CEO and Founder - Maxeler
  Time: 3:00 PM - 3:30 PM
  Session Details

- **Guest Session:** AWS IoT & Xilinx
  Speaker: Richard Elberger
  Partner Solutions Architect, IoT - AWS

  Speaker: Wesley Skeffington
  Principle Architect Industrial & Medical - Xilinx
  Time: 3:00 PM - 3:30 PM
  Session Details

- **Guest Session:** Accelerating Big Data Workload with FPGA
  Speaker: Feng Tian
  CTO - Vitesse
  Time: 3:30 PM - 4:00 PM
  Session Details

- **Guest Session:** The Future of Computing for Bioinformatics Applications
  Speaker: Sunder Parameswaran
  VP Products & Marketing - Falcon Computing
  Time: 4:45 PM - 5:15 PM
  Session Details

- **Guest Session:** Drug Discovery using Molecular Dynamics on Xilinx FPGAs
  Speaker: Vipin Sachdeva
  Principal Investigator - Silicon Therapeutics
  Time: 5:15 PM - 5:45 PM
  Session Details

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Data Scientist / Frameworks | **DAY 2**

This track is intended for data scientists and users for machine learning frameworks who want to learn how and when to target FPGAs to accelerate applications that incorporate AI such as speech recognition, video analytics, big data, networking and more. The Xilinx ML Suite and DeePhi ML tools will be highlighted as means to add machine learning to existing applications targeted for both edge and cloud. FPGA cloud services, environments, framework support and models will be discussed as an overall environment that abstracts hardware complexity for users while retaining performance, low latency, and adaptability for emerging applications using accelerated inference.

12:00 PM - 5:45 PM

- **Session:** Accelerating AI in Datacenters - Xilinx ML Suite Lab
  Speaker: Rahul Nimalyar
  Xilinx
  Time: 12:00 PM - 12:30 PM
  Session Details

- **Guest Session:** IBM PowerAI Vision with Xilinx FPGA Acceleration
  Speaker: Amartey Pearson
  Sr. Technical Staff Member - IBM PowerAI Development
  Time: 12:30 PM - 1:00 PM
  Session Details

- **Guest Session:** Speech Recognition Powered by Xilinx FPGA for Virtual Personal Assistant, NUGU
  Speaker: Minwook Ahn
  Module Leading Developer in ML Infra Lab - SK Telecom
  Time: 1:30 PM - 2:00 PM
  Session Details

- **Session:** Deep Compression and Efficient Speech Recognition Engine (ESE) for LSTM
  Speaker: Jingxiu Liu
  Director of Product Marketing - Xilinx
  Time: 1:00 PM - 1:30 PM
  Session Details

- **Guest Session:** Make the FPGA Disappear Behind the AI
  Speaker: Ludovic Larzul
  Founder & CEO - Mipsology
  Time: 2:15 PM - 2:45 PM
  Session Details

- **Guest Session:** FPGA Acceleration of Apache Spark on the Cloud, Instantly
  Speaker: Dr. Chris Kachris
  CEO - INAccel
  Time: 2:45 PM - 3:15 PM
  Session Details

- **Guest Session:** Turbo Charge Your Insight
  Speaker: Dr. Tanya Roosta
  AI Research - SumUp Analytics
  Time: 3:15 PM - 3:45 PM
  Session Details

- **Session:** Xilinx ML Suite Lab
  Speaker: Kamran Khan
  Product Marketing Manager - Libraries and Software Acceleration
  Time: 4:00 PM - 5:30 PM

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Xilinx Security Design Workshop | **DAY 1**

Derived from the Xilinx Security Working Group series, the XSDW is a special 2-day breakout track at XDF. It brings together Xilinx experts and the Xilinx developer community to discuss the latest security topics in a wide range of commercial markets, including Data Center, Automotive, Industrial and Communications, and provides tips for enhanced security application development.
A secondary registration and acceptance as well as a non-disclosure agreement is required to attend this workshop. Members of this workshop must be accepted to attend prior to the start of XDF.

9:00 AM - 5:30 PM

- **Session:** Introduction to Xilinx Security
  Speaker: Jason Moore
  Director - Core Vertical Market Engineering
  Time: 8:30 AM - 9:00 AM

- **Session:** What's "In the Box" and What's "Out of the Box"
  Speaker: Jason Moore
  Director - Core Vertical Market Engineering
  Time: 9:00 AM - 10:00 AM

- **Session:** Next Generation Security / Survey
  Speaker: Jason Moore
  Director - Core Vertical Market Engineering
  Time: 10:30 AM - 12:00 PM

- **Session:** Zynq UltraScale+ MPSoC Security
  Speaker: Jim Wesselkamper
  Principal Engineer - Core Vertical Market Engineering
  Time: 1:00 PM - 2:00 PM

- **Session:** Zynq UltraScale+ MPSoC Secure Boot
  Speaker: Jim Wesselkamper
  Principal Engineer - Core Vertical Market Engineering
  Time: 2:30 PM - 3:30 PM

- **Session:** Zynq UltraScale+ MPSoC Trusted Execution Environment
  Speaker: Nathan Menhorn
  Staff Applications Engineer - Core Vertical Market Engineering
  Time: 3:30 PM - 4:15 PM

- **Session:** UltraScale and UltraScale+ FPGA Security
  Speaker: Ed Peterson
  Sr. Staff Applications Engineer - Core Vertical Market Engineering
  Time: 4:15 PM - 5:00 PM

- **Session:** Wrap-up / Summary Statements
  Time: 5:00 PM - 5:30 PM

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Xilinx Security Design Workshop | **DAY 2**

12:00 PM - 5:45 PM

- **Session:** All Hands Day 2 Re-Greet
  Time: 10:30 AM - 10:45 AM
- **Session:** Guidance on Essential Security Design Resources / Information
  Speaker: Bryan Penner
  Field Applications Engineer - Xilinx
  Time: 10:45 AM - 11:15 AM
- **Session:** Security Monitor (SecMon) IP
  Speaker: Trevor Hardcastle
  Sr. Staff Applications Engineer - Core Vertical Market Engineering
  Time: 11:15 AM - 12:15 PM
- **Session:** Security in Industrial IoT Applications
  Speaker: Jason Moore
  Director - Core Vertical Market Engineering
  Time: 1:15 PM - 2:15 PM
- **Session:** Security in Automotive Applications
  Speaker: Wes Skeffington
  Principal Architect - Industrial & Medical
  Time: 2:15 PM - 3:15 PM
- **Session:** Security in FPGA as Service (FaaS) Applications
  Speaker: Ed Peterson
  Sr. Staff Applications Engineer - Core Vertical Market Engineering
  Time: 3:45 PM - 4:15 PM
- **Session:** Security in DataCenter Applications
  Speaker: Nathan Menhorn
  Sr. Staff Applications Engineer - Core Vertical Market Engineering

  Speaker: Nick Tausanovitch
  Director - Systems / Solutions Architecture

  Time: 4:15 PM - 5:15 PM
- **Session:** UltraScale and UltraScale+ FPGA Secure Configuration
  Speaker: Ed Peterson
  Sr. Staff Applications Engineer - Core Vertical Market Engineering
  Time: 10:45 AM - 11:15 AM
- **Session:** Funtional and Physical Isolation within the ZynqUltrascale+ MPSoC
  Speaker: Steve McNeil
  Principal Engineer - Core Vertical Market Engineering
  Time: 11:15 AM - 12:15 PM
- **Session:** Zynq UltraScale+ MPSoC Secure Boot
  Speaker: Jim Wesselkamper
  Principal Engineer - Core Vertical Market Engineering

  Speaker: Trevor Hardcastle
  Sr. Staff Applications Engineer - Core Vertical Market Engineering

  Time: 1:15 PM - 3:15 PM
- **Session:** Zynq UltraScale+ MPSoC Enhanced Key Revocation
  Speaker: Nathan Menhorn
  Sr. Staff Applications Engineer - Core Vertical Market Engineering

  Speaker: Ed Peterson
  Sr. Staff Applications Engineer - Core Vertical Market Engineering

  Time: 3:45 PM - 4:15 PM
- **Session:** Secure Storage Using the Zynq UltraScale+ MPSoC Physical Unclonable Funtion(PUF)
  Speaker: Nathan Menhorn
  Sr. Staff Applications Engineer - Core Vertical Market Engineering

  Speaker: Ed Peterson
  Sr. Staff Applications Engineer - Core Vertical Market Engineering

  Time: 4:15 PM - 4:45 PM
- **Session:** UltraScale and UltraScale+ FPGA Tamper Logging and Penalty Response
  Speaker: Ed Peterson
  Sr. Staff Applications Engineer - Core Vertical Market Engineering
  Time: 4:45 PM - 5:15 PM

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ABSTRACTS

Developer Labs and Sessions | **DAY 1**

9:00 AM - 5:30 PM

Amazon EC2 F1 Instances Developer Lab

During this lab you will receive an overview of AWS F1 and SDAccel and step-by-step instructions using Amazon EC2 F1 instances to accelerate your applications. You will also learn how to connect to an F1 instance, experience F1 acceleration, and develop and optimize F1 applications with SDAccel.

Machine Learning for Embedded Workshop

In this interactive lab session you will learn how to build machine learning applications for embedded system using Xilinx end-to-end DNN tool chain. We will guide you to go through the whole process from quantization, through compilation to deployment with Xilinx XCZU2EG or Avnet Ultra96 board. After the workshop, you are able to try your own DNN on Xilinx embedded platform. No prior knowledge of any FPGA or other Xilinx tool is required.

Model-Based Design with Xilinx Model Composer and Simulink (Hands-on Labs)

Xilinx Model Composer, an add-on toolbox for the MathWorks Simulink® environment, enables algorithm engineers to design, simulate and accelerate the path to production on Xilinx devices, without worrying about low-level implementation specifics. With fast simulation speeds, support for frame-based designs, tight integration with Simulink and add-on toolbox features, algorithm engineers can build system-level designs to work at a higher-level of abstraction while moving from their "golden reference" algorithms towards an optimized implementation on Xilinx. In these self-paced labs, you will get a hands-on introduction to Xilinx Model Composer - Learn how to create a frame-based implementation design within Simulink using high-level Xilinx optimized block libraries, import C/C++ functions as custom blocks, experience the benefit of fast simulation speeds for rapid design exploration, automatically generate Vivado HLS synthesizable code from your designs or packaged IP and more!

Using Machine Learning with SDSoC to Create Embedded Vision Systems

An overview of Xilinx machine learning solution, including hardware platform, IP, libraries, tool, documents and design examples to help you build embedded AI products with high productivity. The system integration in both Vivado and SDSoC environment will be covered. We will also unveil some technical details to help you understand how it works and why it works so well.

Introduction to Ultra96 and Xilinx Embedded Software

Introduced at Linaro Connect in March and compliant to the 96-Boards standard from Linaro - The Ultra96 platform is the ideal, low cost community platform for software developers to learn, hands-on, about the power and capabilities of Xilinx's flagship Zynq UltraScale+ platform - a highly adaptable ARM based Heterogeneous SoC. In this session you will get an introduction to the SoC platform, Xilinx's embedded software runtime environment and the Ultra96 platform.

Please note this development kit will be used in all hands-on workshops throughout the two day XDF event - thus this forms a great starter session to your XDF developer experience.

Building Vision System using ML + CV + Sensors w/SDSoC

In this interactive lab session you will learn how to integrate embedded sensors, image processing, and machine learning for embedded devices using the Xilinx SDSoC development environment. We will build a complete end-to-end application to run on the Ultra96 XCZU3EG development platform taking video from a USB webcam, performing image pre-processing and machine learning with hardware-accelerated C++ functions in the FPGA fabric, and interpret the results. No prior knowledge of SDSoC is required.

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ABSTRACTS

Developer Labs and Sessions | **DAY 1**

9:00 AM - 5:30 PM

Introduction to Software Acceleration with SDSoC

The world is changing, solutions need to be developed faster, developers need design flows that enable this accelerated development cycle. Is software or hardware the best place for a specific algorithm? Do you have the right balance of software and hardware expertise in your engineering group? What is that right balance? In this session you will be introduced to Xilinx's SoC development environment for software engineers - namely SDSoC - learning how to leverage the system compiler technology that enables an offload from software to hardware.

Conversation with Xilinx Research Labs

This session is hosted by Xilinx CTO Ivo Bolsens and his team at Xilinx Labs. It is focused on XDF attendees from academia and education, yet open to everyone. Ivo and his team will share their perspective on key technology trends, showcase their own work, and discuss their collaborations including several open source initiatives and books. The team will present open research questions and opportunities for collaboration. There will be ample time for Q&A and discussion.

The topics and initiatives include:

- Research opportunities in machine learning for reduced precision networks enabled by FINN
- P4 programming language for adaptable networking
- RapidWright: Modular pre-implemented methodology and data movement
- PYNQ: New directions in heterogeneous embedded systems development
- Xilinx University Program: trends in modern EE/CS education

Accelerate FPGA Development, test and application deployment natively on AWS EC2 F1

Amazon EC2 F1 allows developers to develop, test and deploy custom FPGA hardware accelerators at scale. Supercharging applications running in the cloud by porting C/C++ code or RTL to custom FPGA hardware acceleration. In this chalk-talk session, we will focus on the benefits of accelerating and scaling applications using Amazon EC2 F1 instances, including a live demo and a follow-on open discussion with the EC2 F1 team.

OpenCV Acceleration

Xilinx reVISION stack includes a range of development resources for platform, algorithm and application development. It includes support for the most popular neural networks including AlexNet, GoogLeNet, VGG, SSD, and FCN. Additionally, the stack provides library elements including pre-defined and optimized implementations for CNN network layers, required to build custom neural networks (DNN/CNN). The machine learning elements are complemented by a broad set of acceleration ready OpenCV functions for computer vision processing. For application level development, Xilinx supports industry standard frameworks and libraries including Caffe for machine learning and OpenCV for computer vision.

This session provide hands-on training of the reVISION stack and leverages the Ultra96 platform to port and accelerate OpenCV functions using SDSoC.

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XILINX

XDF XILINX DEVELOPER FORUM

ABSTRACTS

Developer Labs and Sessions | **DAY 1**

9:00 AM - 5:30 PM

Accelerating Hadoop Map-Reduce on F1 and Achieving 10X Speed-up!

Hadoop's Map-Reduce, because of its resilience, stability and predictability, is a widely adopted paradigm to solve challenges of big-data applications. Almost all major big-data players make use of Map-Reduce framework. However, the generality of map-reduce also comes with its own set of problems. There are serious runtime bottlenecks when data is passed from map stage to reduce stage. It is widely known that these problems when targeted for FPGAs can provide orders of magnitude faster turn-around.

BigZetta's bzAccel product uses existing hooks in Hadoop's framework to offload runtime intensive computations to FPGAs. By working alongside Hadoop, bzAccel removes the runtime bottle-necks and ensures that Hadoop's core strengths like resilience, stability etc. are not compromised. On various big-data benchmarks, Hadoop-with-bzAccel has demonstrated 10-20x speed-up over standalone Hadoop. In this presentation, we will show how BigZetta was able to achieve such dramatic results by making use of SDAccel and F1 machines.

Addressing the Ease-of-Deployment and Monetization Challenges for Cloud and on-premise: How to Further Accelerate the Adoption of FPGAs in Data Centers

Making FPGAs ubiquitously used in data centers requires solutions to be readily usable and purchasable with a pay-per-use model: Software APIs to operate the FPGA functions are critical but quick evaluation and non-disruptive implementation are also key. Paying for FPGA solutions based on usage is fundamental for both the FPGA solution providers and IP providers.

Accelize has developed unique tools and services that address these 2 critical challenges. Stephane will highlight the value of Accelize's FPGA Functions for AWS F1 (Compression, Analytics, Security and Video Transcoding) with its key IP partners, and their ease of use through Accelize's RESTful API. He will then present Accelize's Digital Right Management (DRM) Platform that enables implementation of any business model (Node locked, Floating, time-based, data-based, ...) securely when deploying FPGA functions in the Cloud or on-premise.

AI Developer Lab with Xilinx ML Suite for DC / Cloud

In this lab, developers will gain hands on experience with using the Xilinx ML Suite and how to accelerate inference for machine learning on Xilinx devices.

Python on Zynq UltraScale+ Showcasing OpenCV Libraries

Python is fastest growing language in the software community. Xilinx has developed a framework using Python & Jupyter Notebooks to run on Xilinx's family of SoCs called PYNQ. The PYNQ framework extends the Project Jupyter software stack. It runs on headless Linux on Zynq's processor system, in parallel with overlays in the programmable logic. Overlays are FPGA designs that are domain-specific, yet highly customizable at run-time from software. PYNQ introduces hybrid libraries for packaging overlay bitstreams, Tcl files, drivers, APIs and Jupyter notebooks. The PYNQ framework can be used in concert with Xilinx's reVISION Platfroms, SDSoC and OpenCV. This combination can create a powerful and productive way to implement products for embedded vision - In this session you will get to test drive the experience.

FPGA Accelerated Genomics Analysis

Advances in high-throughput sequencing have created massively increasing data throughput, plunging costs, and the emergence of clinical genomics. As such, the bottleneck has shifted from sequencing itself to the bioinformatics pipeline, thereby driving the demand for new technology development. Current secondary processing solutions are slow, non-scalable and often complicated and cumbersome to use. To address this challenge, we developed DRAGEN, a compact hardware-accelerated platform which is more accurate and orders of magnitude faster than current pipelines. We discuss the usage of FPGA technology at the core of the platform and how it is used to implement acceleration of genomic analysis. We cover the architecture chosen to meet cost and compute requirements for various appliances. We show how the architecture leverages common software and IP across product lineups, and enables extensibility of the platform to new algorithms in genomics and beyond.

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XILINX

Hardware Design | **DAY 2**

12:00 PM - 5:45 PM

FPGA Design with the Cloud From Simple Compliation to Timing Optimization

Plunify Cloud is a product of a partnership between Xilinx and Plunify to enable FPGA design in the cloud. With on-demand hourly compute resources and licenses, what can FPGA designers do to be more productive and improve their development processes?

This presentation talks about ideas, techniques and solutions to leverage on the cloud without becoming an IT expert. The first part talks about the common problems encountered by first time users in the cloud. The second part introduces solutions that can ease the burden on cloud users and the 3rd part describes how a customer can leverage on the cloud not only for daily builds, but also optimize their designs to achieve better quality of results.

HLS Tips and Tricks

Understand the value proposition of Xilinx Vivado high level synthesis, the key concepts and optimizations. During the session the most important optimization techniques are reviewed and illustrated through simple code examples.

RTL Synthesis Methodology (Session 1 & 2)

The session will address synthesis, implementation, timing closure and methodology issues that impacts design closure. The session will review a few of the latest methodology DRCs that were added to Vivado. We will go through a few design guidelines, customer case studies and tips and tricks for design closure including the waiver mechanism. The waiver mechanism allows you to hide non-critical violations in methodology, DRC and CDC reports. Hiding non-critical violations allows you to focus on the few critical violations that will gate design closure. The session will also cover new tool features like Incremental Synthesis. Adopting incremental synthesis feature will reduce your synthesis runtime by almost 40%.

Revision Control Methodology

Revision control should be the foundation of any product development. Preserving the correct files so your project can be faithfully recreate is extremely important. In this session we will cover our recommendations for using revision control systems with Xilinx tools. We will introduce recommendations for RTL projects, Xilinx IP, custom IP, IP Integrator block diagrams, and Vivado output products consumed by other tools.

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ABSTRACTS

Hardware Design | **DAY 2**

12:00 PM - 5:45 PM

Timing Closure Tips and Tricks (Session 1 & 2)

Timing Closure has traditionally been an increasingly complex and iterative process, becoming even more difficult with exponential growth in device sizes and capabilities. Learn how Xilinx automates much of the "heavy lifting" for you with new tools that go well beyond identifying critical paths and instead offer turnkey solutions. We will also introduce new techniques for achieving the maximum performance from Stacked Silicon Interconnect (SSI) devices, enabling you to refocus on building your customized solutions.

Partial Reconfiguration: Methodologies for Creating Reconfigurable Applications

This session provides a look behind the curtain to show the development of the technology empowering SDAccel solutions. The SDAccel environment provides a framework for developing and delivering FPGA accelerated data center applications using standard programming languages. Partial Reconfiguration is the heart, mapping reconfigurable applications into a dynamic workspace. This presentation will illustrate the history of platform development within Xilinx, starting with the fundamental silicon and software technology that makes it all possible. A glimpse into the possible future of platform capabilities will also be shown.

Visual System Integrator (VSI): An Environment for Rapid Development & Integration of Heterogenous Systems

SystemView Inc. offers a tool called Visual System Integrator (VSI) which provides behavioral modeling, simulation and automated design of entire systems of hardware and software running on heterogeneous devices and heterogeneous accelerators. VSI provides run time profiling and metric reporting. VSI, provides users with everything needed for rapid design explorations, behavioral and/or RTL simulations, hardware in loop, external processors, and FPGA design creation of heterogeneous features, including embedded processors, memories and interfaces.

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Embedded System Software | **DAY 2**

12:00 PM - 5:45 PM

Embedded Software Strategy & Development, an Introduction

A beginners guide to Xilinx Embedded software, the ecosystem around Xilinx's embedded software SoC portfolio - including development and open source engagements.

Heterogenous Realtime Software Architecture

Hypervisors are key to enable mixed-criticality systems: a critical workload, typically with real-time requirements, running alongside a larger operating system, such as Linux. The interrupt latency needs to be deterministic, and the boot time of the critical function only a fraction of a second. Hypervisors are also the enabling technology to securely deploy new customers apps at runtime, without affecting system safety.

This presentation will give an overview of hypervisor technologies for Xilinx platforms. It will introduce the most recent developments of the Xen hypervisor, including the "null" scheduler and dom0less, and it will explain how to make use of the new features to best configure Xen for embedded environments.

SoC Platform Management

Platform Management provides common services to Heterogeneous Systems, allowing more time for Application development. Such services include Power Management, Boot and Configuration. This overview describes the structure of Platform Management, how to interface to it, links to additional resources, and recent design applications.

From DC to Daylight, Xilinx RF Solutions for Wired, Wireless and High Frequency Applications

Learn about Xilinx's industry leading Zynq UltraScale+ RFSoC devices with multi-giga-sample direct-RF A/D and D/A converters and Soft-Decision Forward Error Correction (SD-FEC) modules. With this exciting direct RF sampling technology - moving the A/D and D/A conversion process closer to the antenna such that the converter directly samples the RF signal. With this technology, Moore's Law can be applied to frequency selection and down conversion, traditionally implemented using analog signal processing techniques. By allowing analog/RF signal processing to be moved in to the digital domain, a more flexible and programmable solution can be delivered with a dramtically reduced system cost, power and size footprint.

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Embedded System Software | **DAY 2**

12:00 PM - 5:45 PM

Multimedia SoC System Solutions

Xilinx provides comprehensive solutions for users to realize a wide variety of multimedia (Audio, Video and graphics) applications on Xilinx's Zynq® UltraScale+™ MPSoC. The solutions allow users to implement highly custom and optimal solutions for specific applications by mixing high performance hardened multimedia blocks in the processing subsystem (PS) with highly configurable soft Audio and Video IPs implemented in the Programmable Logic (PL). On software front, multimedia blocks e.g. Audio/Video capture, processing, coding, display etc. come with standard software frameworks (V4I2, OpenGL-ES, OpenMax, ALSA and DRM/KMS). For application developers, Xilinx provides gstreamer open-source collaborative solutions which make use of standard driver framework to develop the non-trivial multimedia pipelines. Using gstreamer framework, users can achieve their end application by just describing the data flow which helps shorten the development cycle. Multimedia overview session covers the hardware and software aspect of Multimedia blocks which consist of hardened blocks in Processing subsystem as well as programmable logic IPs. For multimedia application developers, session also covers details about gstreamer framework to help them to develop their real use-case.

Bringing the Benefits of Cortex-M Processors to FPGA

FPGAs enable custom solutions to be created quickly and with a minimal amount of engineering effort. What if you could combine the flexibility of an FPGA with the processing and software ecosystem advantages of a Cortex-M processor? This joint Xilinx and Arm technical presentation will explore how to use Cortex-M processors in Xilinx-based FPGAs, providing guidance on all of the key steps in building a successful FPGA solution: integration, verification, synthesis, and software development leveraging the large Arm-based software development ecosystem.

System Design from Antenna to Digital with Zynq UltraScale+ RFSoC

The quest for increased bandwidth in latest generation wireless, cable access, early warning / radar, and other high performance RF applications imposes challenging demands on power consumption, thermal management and system integration. With multi-channel direct RF-sampling data converters, Zynq® UltraScale+™ RFSoC can connect seamlessly to custom RF front-ends to offer the most flexible, smallest footprint, and lowest power solution to finally deliver on the promise of true software-defined radio (SDR).

This presentation explores the entire signal chain from antenna to digital with the Avnet Zynq UltraScale+ RFSoC Development Kit featuring a 2x2 LTE Band-3 RF front-end card from Qorvo. Advanced techniques for system-level modelling and simulation with tools from MathWorks and Xilinx will illustrate the design process of software-defined radio systems with Zynq UltraScale+ RFSoC from concept to verification.

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Edge Software Development | **DAY 2**

12:00 PM - 5:45 PM

Xilinx Machine Learning Strategies with DeePhi Platform

In this session, you will learn the significantly accelerated Xilinx product roadmap and vision in enabling machine learning designs through recent acquisition of Deephi. We will discuss the overall Machine Learning landscape, key industry challenges, followed by product offering on Machine Learning and Edge Computing from Xilinx. We will also discuss product and technology roadmaps.

Design and Deploy Accelerators for Embedded Vision Systems using Model Composer and SDSoC

In this self-paced lab, you will get hands-on experience with moving from a high-level of abstraction algorithm, captured within the MathWorks Simulink® environment using the Xilinx Model Composer add-on toolbox, towards a live I/O implementation on the Avnet Ultra96 board through integration with the SDSoC development environment.

Accelerating ADAS Computer Vision Application Development at Ford using SDSoC

Embedded Computer Vision technology is used by many Advanced Driver Assistance Systems to offer both safety and convenience features in automobiles. This technology is gaining importance as the number of camera sensors per vehicle continues to increase. This presentation will share insights from how a small team of software engineers at the Ford Research and Innovation Center in Palo Alto accelerated the development of a Computer Vision Application for ADAS using Xilinx SDSoC with reVISION libraries.

Machine Learning for Embedded

In this interactive lab session you will learn how to build machine learning applications for embedded system using Xilinx end-to-end DNN tool chain. We will guide you to go through the whole process from quantization, through compilation to deployment with Xilinx XCZU2EG or Avnet Ultra96 board. After the workshop, you are able to try your own DNN on Xilinx embedded platform. No prior knowledge of any FPGA or other Xilinx tool is required.

Machine Learning for Embedded Deep Dive

In this interactive lab session you will learn how to build machine learning applications for embedded system using Xilinx end-to-end DNN tool chain. We will guide you to go through the whole process from quantization, through compilation to deployment with Xilinx XCZU2EG or Avnet Ultra96 board. After the workshop, you are able to try your own DNN on Xilinx embedded platform. No prior knowledge of any FPGA or other Xilinx tool is required.

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Edge Software Development | **DAY 2**

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Using Machine Learning with SDSoC to Create Embedded Vision Systems

An overview of the Xilinx SDSoC development environment, libraries, and platforms for embedded vision systems with a deep focus on accelerating artificial intelligence using FPGA fabric. We will provide an overview of the development flow using real-world examples showcasing how you can apply Xilinx machine learning technology to your unique applications.

Building Vision System using ML + CV + Sensors /w SDSoC

In this interactive lab session you will learn how to integrate embedded sensors, image processing, and machine learning for embedded devices using the Xilinx SDSoC development environment. We will build a complete end-to-end application to run on the Ultra96 XCZU3EG development platform taking video from a USB webcam, performing image pre-processing and machine learning with hardware-accelerated C++ functions in the FPGA fabric, and interpret the results. No prior knowledge of SDSoC is required.

Expert Panel for Edge Computing: ML, OpenCV, SDSoC, Sensor Fusion

In this session, you will hear Xilinx experts discuss common topics in Machine Learning and Edge Computing development flow. It is also an great opportunity to meet the experts and discuss your questions as the session will resume into an “meet-an-expert” after the panel discussion.

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XDF XILINX DEVELOPER FORUM

ABSTRACTS

Cloud Software Development | **DAY 2**

12:00 PM - 5:45 PM

State of FPGA-based Acceleration

Over the past couple of years, FPGA-based acceleration has matured from a promising concept to a proven solution with compelling results. Hyperscalers are accelerating their own workloads with FPGAs while cloud providers are making FPGAs easily available to app developers. One year ago, AWS made it possible to use the SDAccel Development Environment to create apps for their EC2 F1 instances. Today many developers across different industry segments are targeting FPGA-accelerated platforms. The catalog of FPGA-ready apps is steadily growing with academia joining this trend. This presentation will review the state of FPGA-based acceleration. Come learn about the range of applications and frameworks that have been accelerated in data analytics, genomics, video processing, machine learning, financial technology and security.

Video Acceleration in the Cloud Using FPGAs

The amount of processing needed to run video workloads is growing rapidly. This stems from higher resolutions, higher frames rates, migration to higher bit-depths, and newer more complex codecs like VP9, HEVC and AV1. Considering all of these factors, the industry is facing 10-50x higher demand on its infrastructure compute needs for video workloads. This is happening while the volume of live video streams that require processing is growing exponentially. This session will show how Xilinx FPGAs are the ideal solution to accelerate these workloads. FPGAs offer full flexibility and configurability, while maintaining substantial performance density and performance per watt increases over non-accelerated solutions. Finally, we will show examples of how Xilinx's accelerated video transcoding ecosystem plugs seamlessly and transparently into common video frameworks like FFmpeg.

Converged IO Acceleration Platform

The modern trend towards virtualized and containerized cloud infrastructure with ever increasing demands on features and performance is placing a significant load on server CPUs. This coupled with emerging diverse compute workloads such as machine learning, big data analytics, and streaming video requires an intelligent, programmable and scalable converged IO acceleration platform

In this session we will highlight our adaptable and high performance FPGA-based SmartNIC network processing platform for offloading key network virtualization functions enabling scalable thin-hypervisor and bare-metal infrastructure. The proposed platform is adaptable and extensible allowing flexible addition of key networking functionality such as custom packet processing, virtual switching offload, and security as well as inline interfacing with key compute functions including video, data analytics, and machine learning. The platform leverages Xilinx state-of-the-art IP portfolio and industry leading tools including P4-SDNet.

Empowering Software Developers - Scaling FPGA Application Development

FPGAs have been established in the industry as mainstream acceleration devices and Xilinx is leading the industry in FPGA as a Service (FaaS) with our flagship deployment in AWS F1 and with most major cloud providers. FPGAs true potential can be reached with a rich ecosystem of accelerated applications. Historically FPGAs have been programed using Hardware Description Languages and were considered difficult to use by software developers. But this paradigm is rapidly changing. Xilinx has been investing substantially to create a rich environment for enabling far more developers to tap into the power of FPGA acceleration. For software developers we are offering a native experience with vastly improved Ease of Use and for those with prior FPGA experience we are offering a whole new level of development productivity. Come learn about our vision for software programmability, our progress and roadmap, and why, as an active or potential FPGA application developer, this is important for you.

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Cloud Software Development | **DAY 2**

12:00 PM - 5:45 PM

The Nuts & Bolts of Computational Storage Platform

More than 90 percent of the data in today's world was generated in the last two years alone. To keep up with the exponential increase in the corresponding compute needs, new data centers are being created and new technologies invented every day. A key trend is the emergence of workload acceleration by means of offload engines to augment the CPU. While offloading CPU using workload specific accelerators is not new, little has been done to optimize the vast potential of bringing compute closer to the data. This presentation focuses on a computational storage development platform that takes advantage of keeping hardware programmable FPGA fabric in a tight loop with flash based NVMe storage, while presenting the developer with the same application view. Developers get to understand the nuts and bolts of the platform that can help them achieve an order of magnitude of acceleration for applications that can take advantage of near-data-compute.

Developing Computational Storage Applications using SDAccel

Data is growing at a rapid pace. With the scale of growth of data, comes the need for powerful analytics closer to where the data resides. Computational Storage platform solves that problem by unleashing TeraOps of computation power of FPGA next to SSD. In this talk, we will highlight how you can create these powerful analytics applications usingon our computational storage platforms using SDAccel. We will also present how it is easy to port existing applications running on FPGA on cloud like AWS F1 to these platforms and showcase additional acceleration of these applications leveraging the FPGA next to SSD.

Fundamentals of FPGA based Acceleration

FPGA-based acceleration has emerged has the hottest trend in high-performance computing. In domains as varied as machine learning, video processing, fintech, genomics or database acceleration, developers are turning to FPGA to accelerate compute-intensive and performance critical workloads. But what exactly is FPGA-based acceleration? How does it work and why can it provide processing speeds up to 100x faster than conventional compute instances? This session will focus on the fundamentals of FPGA-based acceleration. It will provide a down to earth explanation of the technology and its inner workings. Attendees will gain practical knowledge about what impacts performance the most, which workloads are best suited for FPGA-based acceleration and, as importantly, which ones are not.

Using SD Accel for Host and Accelerator Code Optimizations

SDAccel is a complete integrated development environment (IDE) used to develop FPGA-accelerated applications. It offers all the features of a standard software development environment: an optimized compiler for host applications, cross-compilers for the FPGA, robust debugging environment to help identify and resolve issues in the code, and performance profilers to identify bottlenecks and optimize the code. The host application is developed in C/C++ and uses standard OpenCL API calls to interact with the FPGA device and the accelerated functions. The FPGA accelerated functions can be modeled in either RTL, C/C++ or OpenCL C. This presentation focuses on the most important performance optimization considerations for high-throughput FPGA-accelerated applications. This includes, host program design, accelerator implementation, and especially the interconnect framework around DDR memory, AXI, and PCIe characteristics.

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Cloud Software Development | **DAY 2**

12:00 PM - 5:45 PM

Best-in-Class Video Compression Developed with High Level Synthesis and SDAccel

NGCodec has developed industry leading HEVC and VP9 video compression engines on VU9P FPGAs. Running as accelerators on a PCIe card, these engines can completely offload video encoding from a CPU, resulting in dramatic cost savings and video quality improvement. We will describe the architecture, performance and design methodology of these products. We will discuss our experience using High Level Synthesis and SDAccel as major components of our design process.

Building and Scaling FPGA Accelerated Applications for Cloud Computing

As Moore's Law continues its march towards the atomic scale and applications demand more performance and capability than ever before, FPGAs have become the new canvas on which to build accelerated applications for the data center era. From deep learning to real time encoding, organizations across every major industry are building next generation applications that depend on the power FPGAs. In this talk, Nimbix will discuss how application developers and ISVs can create, develop and monetize applications in the cloud powered by Xilinx FPGAs. Additionally, Nimbix will discuss how its award-winning cloud platform, JARVICE, seamlessly scales applications across both the cloud and private FPGA-powered edge datacenters around the world.

Building Next-Generation Accelerated Video and Machine Learning Software Solutions Running on the Xilinx Virtex UltraScale+

Skreens has built a platform that adds a suite of video and machine learning processing functions on top of the Xilinx environment, accessible via a RESTful API. Skreens enables a single developer-friendly workflow to decode multiple video and content feeds, integrate machine learning models and third-party integrations such as Watson and IFTTT, compile a powerful end-user experience including with event-specific content overlays, and encode the resulting feed – all at ultra low latency. Skreens offers the power of a next-gen production studio, accelerated by FPGAs, and accessible via API FPGA accelerator cards or public cloud UltraScale+ FPGA instances.

The result is a powerful but user-friendly developer system – akin to what Windows offered when built on top of MS-DOS. This presentation will detail how developers can use Skreens to quickly ramp-up and deploy new video intensive software applications for the FPGA, integrate machine learning into their applications right out of the box, and add ultra-low latency interactivity to traditionally linear end-user experiences.

FPGAs - Moving Computation to the Data

Massive amounts of data are being consumed and processed to drive business. The exponential increase in data has not been matched by the computational power of processors. This has led to the rise of accelerators. However, big data algorithms for ETL, ML, AI, and DL are evolving rapidly and/or have significant diversity. These moving targets are poor candidates for ASICs, but match the capabilities and flexibility of FPGAs. Furthermore, FPGAs provide a platform to move computation to the data, away from the CPU, by providing computation at line rate at the network and/or storage. Bigstream is bridging the gap between high-level big data frameworks and accelerators using our Hyper-acceleration Layer built on top of SDAccel. In this talk, we will describe the Bigstream Hyper-acceleration that automatically provides computational storage acceleration for big data platforms with zero code change.

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Cloud Software Development | **DAY 2**

12:00 PM - 5:45 PM

API for Real Time / Dynamic Image Processing

CTAccel was formed in 2016 by a team of FPGA researchers and engineers, most of them had more than 10 years of FPGA development experience. It now has 47 full-time employees based in Shenzhen, China. By leveraging FPGA-based computing technology, CTAccel Image Processing Accelerator (CIP) enables our data center customers to achieve high throughput, low and deterministic latency image processing. The image processing capabilities supported by CIP include jpeg codec, webp encode, lepton codec, resizing/crop. These functions are widely used in thumbnail generation, image transcoding and lossless image compression. The accelerated functions have been seamlessly integrated into OpenCV and ImageMagick which are widely used for data center image processing by Internet companies. Dozens of Xilinx FPGA based CIP accelerator solution has been deployed in Chinese Internet giants, some of these have been in continuous operation for more than a year. In the session, Harry will introduce CTAccel's CIP solutions and some of its successful cases.

Computational Storage - Acceleration Through Intelligence & Agility

Doing more with less is the name of the game when it comes to data center infrastructure scalability, especially when looking at Flash as it becomes the dominant storage media for data-driven applications. Following the principles of intelligence and agility, Computational Storage is today rapidly evolving to meet ever-changing customer needs. It can then handle rapidly expanding demands from applications such as databases, analytics, financial technology, content delivery networks, artificial intelligence, and machine learning, to maximize the benefits of flash deployments.

SDAccel Development Environment: FPGA Acceleration Performance and Ease of Use Aren't Mutally Exclusive

SDAccel is Xilinx's Development Environment for designing, verifying and implementing programs based on the OpenCL framework for heterogenous parallel computing. It offers a powerful combination of performance, ease-of-use, portability, and flexibility to enable the acceleration of applications using heterogenous CPU/FPGA platforms for a wide range of applications. In this talk, we will discuss how SDAccel makes it easier for the developer to create FPGA-accelerated designs without having to sacrifice performance. Additionally, we will describe how we are leveraging SDAccel at BlackLynx to accelerate our heterogeneous computing acceleration flows at the edge, in the data center, and in the cloud.

AWS IoT & Xilinx

The Industrial Internet of Things (IIoT) is rapidly accelerating the opportunity for cloud connected and collaborative control systems that can unlock the next set of capabilities around industrial assets. As IIoT implies a level of connectivity and collaboration of the traditional edge platforms with cloud systems it is logical product evolution for industrial control system providers to find a solution that allows them to securely and quickly tie into existing cloud infrastructures such as AWS to accelerate their IIoT strategies.

In this session AWS will provide an overview of their IoT Edge offerings providing technical overview, dependencies, and how they interact for the AWS IoT Core, a:FreeRTOS, AWS Greengrass, and Amazon SageMaker offerings. Within a:FreeRTOS the session will define how the offering is a superset of functionality that sits on top of the FreeRTOS kernel include a live demonstration showing a:FreeRTOS on a Xilinx platform collaborating with the AWS IoT Cloud.

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Cloud Software Development | **DAY 2**

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AWS IoT & Xilinx

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Accelerating Big Data Workload with FPGA

We designed a new join algorithm to accelerate a massive parallel processing data warehouse using off-board FPGA. FPGA hardware resource is not pre-empted, thus can be shared by many concurrent queries. For some complex SQL queries we achieved 5x performance improvements. The product is available on AWS F1 or Nimbix.

The Future of Computing for Bioinformatics Applications

By 2025, Genomics is projected to produce 40 exabytes of data annually as the latest genomic sequencers generate 2 or more terabytes of data daily. More data opens the opportunity to improved patient care with a caveat. Bioinformaticians and researchers face the dual challenge of having to accelerate workloads to achieve quick and timely results while performing cost-effective analysis. Falcon Computing's solution leverages Xilinx FPGAs to provide a fast, automated and cost-effective framework to accelerate genomics pipelines for secondary sequencing analysis.

In this talk you will learn about:

- Unique challenges in the field of computing for Genomics
- Falcon Computing Genomics Acceleration Platform for industry standard GATK secondary sequencing with Xilinx FPGAs on both private and public clouds
- Customer success stories from world class institutions paving an accelerated path to precision medicine and improved patient care

Drug Discovery using Molecular Dynamics on Xilinx FPGAs

Drug discovery is challenging and expensive. Silicon Therapeutics (STX) uses an RBFE protocol based on all-atom MD simulations running on GPUs as part of the lead optimization pipeline. The two critical bottlenecks are throughput and timescale. We propose to address both problems by accelerating these simulations with Xilinx-based FPGA clusters. As part of this work, we have ported and optimized a mini molecular dynamics application written in OpenCL to utilize Xilinx FPGAs in addition to Nvidia GPUs for some of the time-consuming kernels, and we have obtained promising results. These are the first steps toward running a full MD pipeline running on FPGAs. Beyond utilizing a single FPGA, we aim to harness multiple FPGAs for a single molecular dynamics simulation. Our overall goal is to a create a commercial-quality pipeline utilizing a FPGA rack for running long-timescale MD simulations which will be highly useful to our internal drug discovery efforts.

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Data Scientist / Frameworks | **DAY 2**

12:00 PM - 5:45 PM

Accelerating AI in Datacenters - Xilinx ML Suite Lab

In this talk Xilinx will describe the deep neural network (DNN) processor innovations for Xilinx FPGAs for use in datacenter and cloud environments. The talk will cover hardware architectural details which enable high performance, low latency DNN acceleration, and the software stack which allows users easily deploy trained network models on Xilinx FPGAs for their inference applications.

IBM PowerAI Vision with Xilinx FPGA Acceleration

PowerAI Vision makes computer vision with deep learning accessible to any subject matter expert without a need for programming or data science skills. On accelerated IBM® Power Systems™, you can label, train, and deploy your Vision models all within a single intuitive interface.

Traditionally, computer vision Object Detection inferencing has relied on GPUs or specialized hardware. However with the advent of the Xilinx ML Suite, we can now easily do inferencing at scale leveraging a Xilinx FPGA.

In this talk, we will preview how IBM was able to incorporate the Xilinx ML Suite into a preview version of the PowerAI Vision software and drive performant object detection inference on a user trained model leveraging the Xilinx FPGA Acceleration Hardware in a Power Systems™ server.

Speech Recognition powered by Xilinx FPGA for Virtual Personal Assistant, NUGU

Rapid proliferation is shown of voice interaction capabilities provided by smart speaker like Alexa and Google Assistant in recent two or three years. These provide the ability to speak to your devices, and make them understand and react what you're asking. This is very different from the conventional visual user experience from smartphone, and has a possibility to give a new, and easy-to-use way of interaction between human and machine. 2016, SK Telecom launched a smartphone called NUGU. In this talk, we will introduce a FPGA-based inference accelerator, which can multiply the number of service channels of NUGU more than by three times in the same machine.

Deep Compression and Efficient Speech Recognition Engine (ESE) for LSTM

In this talk Xilinx will describe the software and hardware co-design flow for RNN(LSTM) acceleration. Deephi ESE is an efficient end-to-end automatic speech recognition (ASR) engine, containing pruning, quantization, compilation and FPGA inference. Detail information on how to deploy LSTM IP on AWS/Ali/Huawei cloud and what kind of performance can be expected will be elaborated in detail. Some LSTM IP architecture information will also be shared firstly in public with many details.

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XILINX

Data Scientist / Frameworks | **DAY 2**

12:00 PM - 5:45 PM

Make the FPGA Disappear Behind the AI

Ludovic Larzul, Founder and CEO of Mipsology, has worked more than 20 years on FPGAs and delivered the largest FPGA-based supercomputers. Ludovic will present the reason why FPGAs are ideal to accelerate neural networks in data centers. He will discuss the rational and efforts that led to the development of Zebra on Xilinx FPGA. Zebra is so easy to use that teams developing AI applications can use FPGA without knowing a single thing about them, and don't have to modify any of what they built for CPU or GPU.

Ludovic will disclose the results and performance for the newest and most powerful Xilinx-based boards available today, as well as some hints for the future of AI on FPGAs.

FPGA Acceleration of Apache Spark on the Cloud, Instantly

InAccel provides high performance accelerators for cloud application based on novel hardware reconfigurable engines as IP blocks. The hardware accelerators can be deployed in the cloud, like Amazon AWS, using the f1 accelerators and can be integrated to widely used frameworks like Spark. The main novelty is that the users do not need to change the original code as the accelerators are deployed as software packages. In this talk we will show how machine learning applications (e.g. logistic regression and K-means), based on Spark, can be accelerated by 3x-10x using hardware accelerators that are deployed in the Amazon AWS using f1 accelerators without any changes on the Spark code. InAccel provides all the required APIs for the integration on Spark using Java, Python or Scala. The utilization of hardware accelerators can also be used to reduce the OpEx as less resources and less time is required for the processing of the data.

Turbo Charge Your Insight

Based on the success of its technology offering to Fortune 500 partners, SumUp Analytics developed Nucleus, an AWS F1-powered SaaS for identifying, extracting and analyzing critical information from unstructured text. Leveraging Xilinx FPGAs, SumUp's proprietary technology allows near real-time analysis for many critical tasks in the finance vertical that we serve: topics extraction, summarization, sentiment & consensus analysis and content recommendation, across multiple formats and languages.

The artificial intelligence at the core of Nucleus is a proprietary Adaptive Compressed Sensing model (ACS). ACS provides an efficient and comprehensive combination of words that maximizes information retrieval across documents and allows users to organize large corpuses of text in an interpretable way for their purpose. ACS was originally developed in Python and is now being implemented on FPGA on AWS F1 for further acceleration. We have seamlessly integrated Xilinx high-performance GEMX SDx library with our Python-based Nucleus analytics module. The FPGA-accelerated ACS allows our clients to analyze data ultrafast to deliver insights on-the-fly.

Initially, we are focusing on providing services to finance professionals, who typically spend 30% of their day, searching for meaningful information in unstructured data. Other vertical markets, such as, government intelligence, law, consulting, education, energy and healthcare remain promising areas for long-term user growth.

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